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Research Article

Uncovering the Role of Crystal Phase in Determining Nonvolatile Flash Memory Device Performance Fabricated from $MoTe_2$-Based 2D van der Waals Heterostructures

Yunpeng Xia,◆ Jiajia Zha,◆ Haoxin Huang, Huide Wang, Peng Yang, Long Zheng, Zhuomin Zhang, Zhengbao Yang, Ye Chen, Hau Ping Chan, Johnny C. Ho, and Chaoliang Tan*

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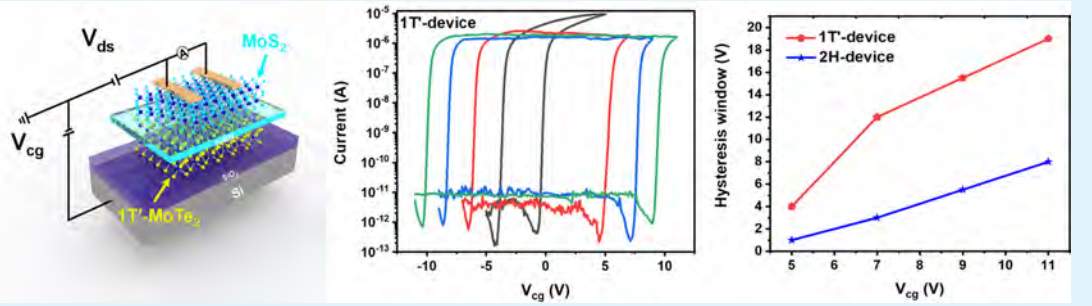

ABSTRACT: Although the crystal phase of two-dimensional (2D) transition metal dichalcogenides (TMDs) has been proven to play an essential role in fabricating high-performance electronic devices in the past decade, its effect on the performance of 2D material-based flash memory devices still remains unclear. Here, we report the exploration of the effect of $MoTe_2$ in different phases as the charge-trapping layer on the performance of 2D van der Waals (vdW) heterostructure-based flash memory devices, where a metallic 1T′-$MoTe_2$ or semiconducting 2H-$MoTe_2$ nanoflake is used as the floating gate. By conducting comprehensive measurements on the two kinds of vdW heterostructure-based devices, the memory device based on MoS_2/h-BN/1T′-$MoTe_2$ presents much better performance, including a larger memory window, faster switching speed (100 ns), and higher extinction ratio (10^7), than that of the device based on the MoS_2/h-BN/2H-$MoTe_2$ heterostructure. Moreover, the device based on the MoS_2/h-BN/1T′-$MoTe_2$ heterostructure also shows a long cycle (>1200 cycles) and retention (>3000 s) stability. Our study clearly demonstrates that the crystal phase of 2D TMDs has a significant impact on the performance of nonvolatile flash memory devices based on 2D vdW heterostructures, which paves the way for the fabrication of future high-performance memory devices based on 2D materials.

KEYWORDS: *crystal phase, $MoTe_2$ nanosheets, 2D van der Waals heterostructures, flash memory devices, floating gate*

1. INTRODUCTION

With the silicon (Si)-based transistors approaching their physical limit, finding a new material system to extend Moore's law becomes the top priority.[1,2] The advancement of two-dimensional (2D) materials in the last decade provides a promising solution in virtue of their unique properties including the immunity to surface-induced performance degradation, facile heterostructure construction, and high compatibility with other materials.[3−6] Owning to their fascinating properties, 2D materials have shown great promise in the fabrication of various high-performance electronics/optoelectronics including field-effect transistors (FETs), phototransistors, and infrared photodetectors.[7−14] On the other hand, the flash memory device is at the cutting edge in transistor density by virtue of its facile extension in the vertical dimension and drives the development of advanced nonvolatile memory applications.[15−17] Especially in today's information age, further improvement of flash memory performance is imminent, and 2D materials and their van der Waals (vdW) heterostructures could be promising candidates for the construction of high-performance flash memory devices.[18−26] As a typical example, Bertolazzi et al. designed a nonvolatile flash memory cell based on a MoS_2/HfO_2/graphene heterostructure.[18] In the same year, Sup Choi et al. demonstrated the ultrathin heterostructured flash memory devices with the structure of MoS_2/h-BN/graphene and

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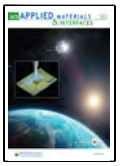

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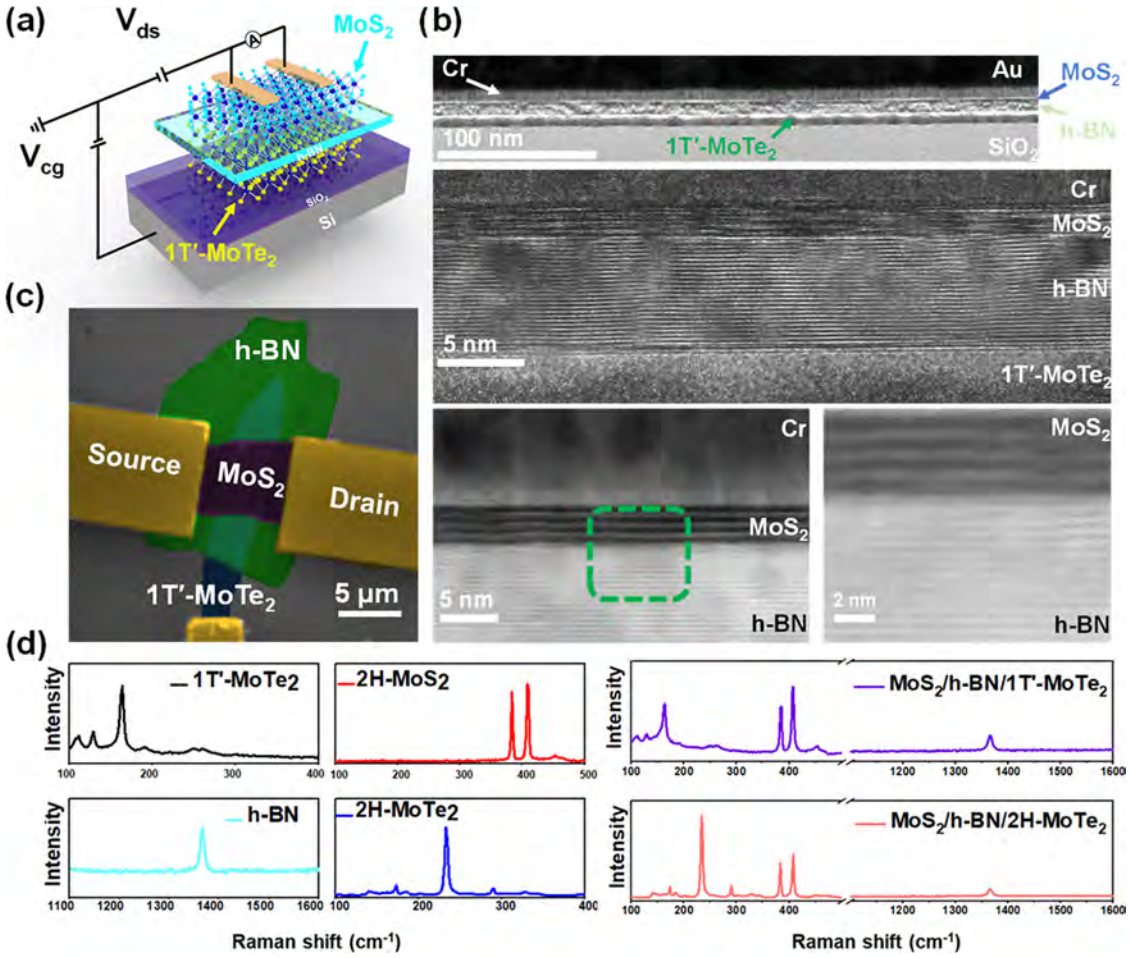

Figure 1. Nonvolatile flash memory device based on the 2D vdW heterostructure. (a) Schematic diagram of the device with 1T′-$MoTe_2$ as the floating gate layer. (b) High-resolution transmission electron microscopy (HRTEM) and scanning transmission electron microscopy (STEM) images of the different layers of the 1T′-device. (c) False-color SEM image of a typical 1T′-device; different layers of the device are indicated in different colors. (d) Raman spectra of the vdW heterostructures for 2H- and 1T′-devices.

graphene/h-BN/MoS_2, respectively.[19] However, considering the commonly used benchmarks, including extinction ratio, switching speed, retention time, and cycle durability, there is still much room for performance improvement in flash memory devices based on 2D materials.[22]

In recent years, the study on the phase engineering of transition metal dichalcogenides (TMDs) endows them with new opportunities to construct advanced electronics/optoelectronics since most TMDs (e.g., MoS_2, WS_2, $MoSe_2$, WSe_2) can crystalize into the common allotropic phases include hexagonal (2H), rhombohedral (3R), octahedral (1T), and distorted octahedral (1T′).[7,27−34] For example, the local phase transition of TMD nanosheets has been applied to realize the ohmic contact in MoS_2- and $MoTe_2$-based FETs and improve the photocurrent in MoS_2-based photodetectors.[35−37] In addition, phase engineering of TMDs (especially for MoS_2, WSe_2, and $MoTe_2$) has been widely used for fabricating advanced memory devices recently. For example, Cheng et al. observed the memristive behavior of the exfoliated metastable 1T-MoS_2-based memristors.[38] In 2018, Rehn et al. theoretically demonstrated the potential of monolayer $MoTe_2$ for phase-change memory with low energy consumption.[39] Then, Hou et al. reported a nonvolatile memory device on the basis of the strain-induced phase changes of the $MoTe_2$ channel in 2019.[40] Moreover, Zhang et al. realized the vertical resistive random access memory (RRAM) devices based on phase transition of 2D $MoTe_2$ and $Mo_{1-x}W_xTe_2$ induced by an electric field.[41] Although there are a few reports about the integration of TMDs in different phases to realize flash memory devices, how the crystal phase of 2D TMDs will affect the performance of the nonvolatile flash memory cells still remains unexplored so far. It is worth pointing out that the metastable nature of metallic 1T/1T′ phases significantly limits the application of most metallic TMDs in electronic and optoelectronic devices since they will easily restore back to the 2H phase under mild treatments (e.g., mild thermal annealing).[42] Promisingly, for $MoTe_2$, both its semiconducting (2H) and metallic (1T′) phases exhibit high stability at ambient conditions, and thus it could be potentially used to study the impact of the crystal phase on various electronic/optoelectronic devices.[39,40,43]

In this work, we first report the comprehensive exploration of the crucial role of the crystal phase of $MoTe_2$ as the charge-trapping layer in flash memory devices based on 2D vdW heterostructures. Specifically, flash memory devices based on MoS_2/h-BN/1T′-$MoTe_2$ and MoS_2/h-BN/2H-$MoTe_2$ vdW heterostructures have been fabricated on the SiO_2/Si substrate, in which 2H-MoS_2 was used as the channel material, h-BN served as the tunnel dielectric, and the metallic 1T′-$MoTe_2$ and semiconducting 2H-$MoTe_2$ were used as the charge-trapping layers. Beneath 1T′-/2H-$MoTe_2$, SiO_2 served as the

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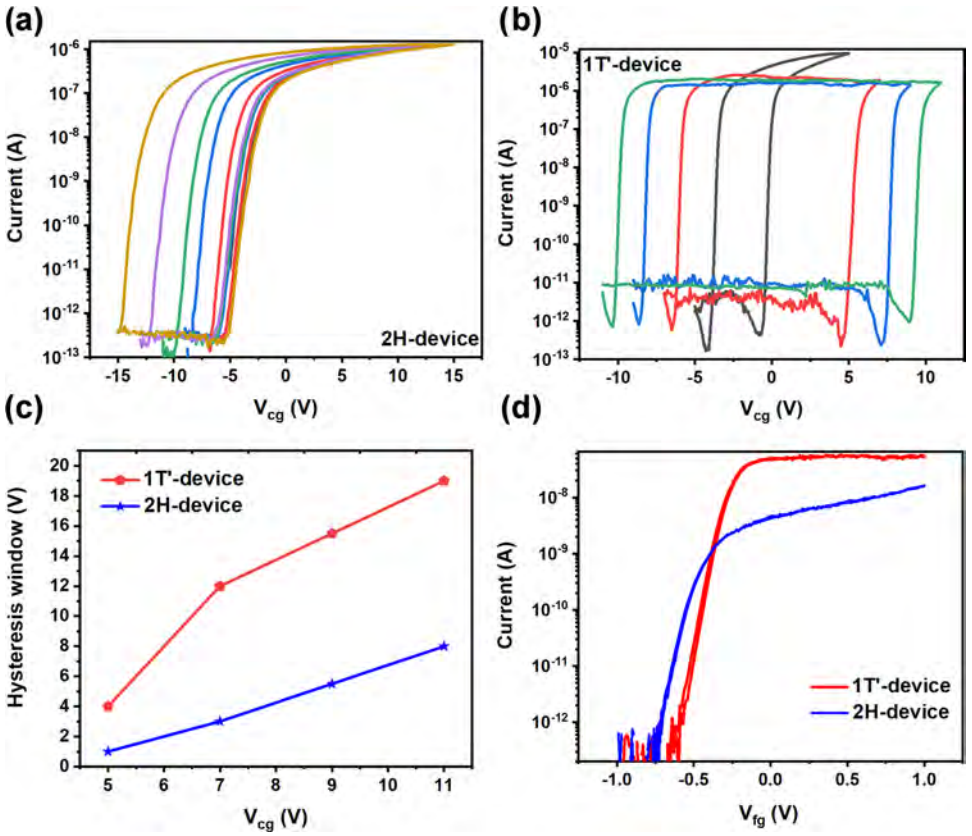

Figure 2. Electrical performance of 2H- and 1T′-devices. (a) Transfer curves of the 2H-device under the bias of 100 mV with the range of V_{cg} increase from ±5 to ±15 V in steps of 2 V. (b) Transfer curves of the 1T′-device under the bias of 100 mV with the range of V_{cg} increase from ±5 to ±11 V in steps of 2 V. (c) Hysteresis window of 2H- and 1T′-devices under different maximum V_{cg}. (d) Transfer curves of 2H- and 1T′-devices under the bias of 100 mV by sweeping the floating gate voltage (V_{fg}) in the ±1 V range on the charge-trapping layers.

gate oxide, and heavily doped Si was used as the control gate. In comparison with its semiconducting counterpart, using the 1T′-$MoTe_2$ nanoflake as the floating gate layer can significantly improve the performance of the fabricated flash memory device, which is much better than that of the device based on the 2H-$MoTe_2$-based heterostructure. The overall performance of the 1T′-$MoTe_2$-based memory cell is even superior to those 2D flash memory devices using graphene as the floating gate.[22,41] In addition, the resistance states of this device can also be programmed by an optical pulse. The MoS_2/h-BN/1T′-$MoTe_2$-based flash memory cell with ultrafast switching speed (100 ns), high extinction ratio (10^7), large memory window, and long cycle and retention stability broaden the way for future high-performance and multifunctional 2D flash memory devices.

2. RESULTS AND DISCUSSION

2.1. Fabrication and Characterization of the Flash Memory Devices. The MoS_2/h-BN/1T′-$MoTe_2$ heterostructure was stacked via a dry transfer method step by step on the SiO_2/Si substrate. Figure 1a shows the schematic illustration of this memory device based on the MoS_2/h-BN/1T′-$MoTe_2$ heterostructure (denoted as the 1T′-device); the bottom layer of the structure is a multilayer 1T′-$MoTe_2$ nanoflake, which serves as the floating gate in the flash memory cell. In the middle, it is the tunnel dielectric h-BN nanoflake, and the semiconducting 2H-MoS_2 nanoflake serves as the channel on the top. The memory device was fabricated by defining the source/drain electrodes via the standard electron beam lithography (EBL), followed by the thermal evaporation of chromium and gold (Cr/Au: 8/60 nm). The Si heavily doped in p-type at the bottom is used as the control gate, which is covered by 50 nm SiO_2 as the gate oxide. Figure 1c shows the false-color scanning electron microscopy (SEM) image of a typical memory device, where the multilayer 1T′-$MoTe_2$ nanoflake marked in dark blue was directly exfoliated onto the SiO_2/Si substrate by a conventional mechanical exfoliation method. The multilayer h-BN nanoflake marked in green and the few-layer MoS_2 nanoflake marked in purple were stacked in sequence via a dry transfer method. The yellow regions in Figure 1c denote the deposited electrodes. In the control group, the flash memory device based on the MoS_2/h-BN/2H-$MoTe_2$ heterostructure (denoted as 2H-device) was fabricated by the same process except for the 1T′-$MoTe_2$ charge-trapping layer, which was substituted by the mechanically exfoliated 2H-$MoTe_2$ nanoflake. The fabrication details of these devices are illustrated in Figure S1 (see the Supporting Information). The thicknesses of MoS_2 and h-BN are about 6.5 and 8.8 nm, while the thicknesses of the floating gate layer are in the range of 15−17 nm.

For the high-performance 1T′-device, we use high-resolution transmission electron microscopy (HRTEM) and scanning transmission electron microscopy (STEM) to characterize the quality of the cross section of the fabricated device in the range of tens of nanometers. In Figure 1b, the first two HRTEM images demonstrate the flat interfaces between these vdW materials in this device, suggesting the high quality of the fabricated heterostructures. The last two STEM images at the

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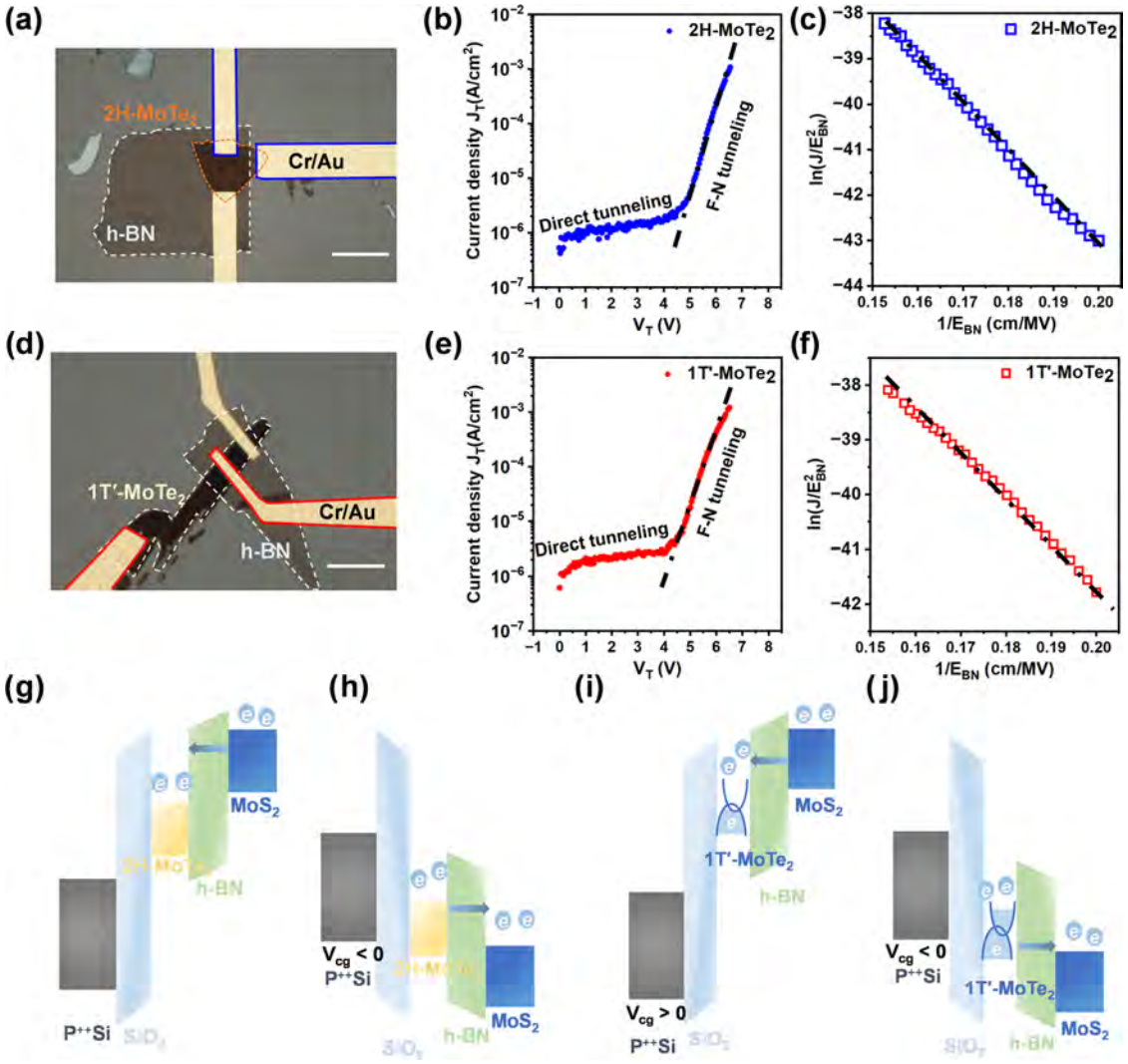

Figure 3. Working mechanism behind the electrical performance of 2H- and 1T′-devices. (a) Optical image of the 2H-$MoTe_2$/h-BN device. (b) Measured tunneling current density J_T as a function of the applied voltage V_T in the 2H-$MoTe_2$/h-BN device in the forward direction. (c) F−N plot of the measured current density of the 2H-$MoTe_2$/h-BN device. (d) Optical image of the 1T′-$MoTe_2$/h-BN device. (e) Measured tunneling current density J_T as a function of the applied voltage V_T of the 1T′-$MoTe_2$/h-BN device in the forward direction. (f) F−N plot of the measured current density of the 1T′-$MoTe_2$/h-BN device. (g) Positive pulse and (h) a negative pulse on the control gate. The energy band diagram of the 1T′-device by applying (i) a positive pulse and (j) a negative pulse on the control gate.

atomic scale indicate the low defect densities at the atomically flat interlayer interface. The energy-dispersive spectrometry (EDS) mapping provides further evidence for the clean interfaces between these vdW materials (Figure S2). The high quality of the fabricated heterostructure eliminates the effects of other factors on the device's performance and lays the foundation for its ultrafast switching speed.[22,45,46]

Figure 1d shows the Raman spectra measured in MoS_2/h-BN/1T′-$MoTe_2$ and MoS_2/h-BN/2H-$MoTe_2$ heterostructures. All of the results are consistent with the previously reported literature, which indicates the purity of each component.[9,47,48] In addition, the thicknesses of different materials in a typical device were measured by the atomic force microscope (AFM). The selection of the thickness of the tunnel dielectric h-BN nanoflake is a trade-off balance between the switching speed and the retention stability.[23] In order to ensure the tunneling efficiency of carriers and charge storage stability, the thickness of the used h-BN layer should be controlled in the range of 8−11 nm based on our experimental results. Specific thickness values for each layer of typical 1T′- and 2H-devices are shown in Figures S3 and S4, respectively.

2.2. Electrical Performance of 1T′- and 2H-Devices.

Figure 2a shows the transfer curves of the 2H-device in different control gate voltage (V_{cg}) ranges. As the absolute values of the control gate voltage increase from 5 to 15 V, the hysteresis window extracted from the transfer curves increases accordingly. The results indicate that 2H-$MoTe_2$ could effectively serve as a charge-trapping layer. The physical mechanism behind this phenomenon is ascribed to the tunneling of charged carriers through the h-BN layer between the semiconducting channel and the floating gate layer. Charge storage and loss in the floating gate layer induced by an external electric field results in the hysteresis window in the transfer curves. Figure 2b shows the transfer curves of the 1T′-device in different control gate voltage ranges. Compared with the 2H-device, the 1T′-device shows a larger hysteresis window under the same control gate voltage and keeps an obvious memory window at a smaller control gate voltage.

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Extrapolation in the linear region method is used to extract the threshold voltages in the forward/backward sweeping directions.[49] When the control gate voltage is in the range of −11 to +11 V, the memory window width (ΔV) of the 1T′-device is approximately larger than 19 V. The comparison of the memory window widths for 2H- and 1T′-devices is shown in Figure 2c. The result reveals that the 1T′-device always presents a larger ΔV than the 2H-device under the same control gate voltage. The memory window usually indicates the storage capacity of the charge-trapping layer in flash memory devices.[22,44] A larger ΔV corresponding to a more significant shift in the threshold voltage means more charged carriers can be stored in the charge-trapping layer, which also suggests a better ability to store information for practical applications.[22,44] We use the following formula to calculate the stored charge density in 2H- and 1T′-$MoTe_2$ floating gate layers

$$\rho = \frac{\Delta V \times C_{CG-FG}}{q} \tag{1}$$

$C_{CG\text{-}FG}$ represents the dielectric capacitance between the floating gate and the control gate, i.e., the capacitance of 50 nm SiO_2 (6.9×10^{-8} F cm^{-2}).[22] And we can calculate that when V_{cg} = 11 V, $\rho_{2H} = 3.45 \times 10^{12}$ cm^{-2} and $\rho_{1T'} = 8.19 \times 10^{12}$ cm^{-2}. It means that the stored charge density in the 1T′-$MoTe_2$ floating gate is considerable. Meanwhile, the higher density obtained in the 1T′-device than in the 2H-device confirms the larger memory window at the same control gate sweeping range. The memory window relates to the read margin in floating gate memory devices and can be an important figure of merit to evaluate our 1T′-device performance among other 2D floating gate memory devices.[18,19,44,50] As shown in Table S1, we summarized the ratio of the memory window range to the sweeping range in our devices with those reported by others; the large value obtained in the 1T′-device demonstrates the superiority of the 1T′-$MoTe_2$ nanoflake as the floating gate layer in the 2D floating gate memory device.

Figure 2d shows the transfer curves of the 2H- and 1T′-devices under the 2H- and 1T′-floating gate voltage control. The near-zero hysteresis window in the obtained results indicates a low trapped charge density at the MoS_2/h-BN interface, and its effect on the performance of the device is trivial. It also proves the high interface quality of these stacked vdW heterostructures. Figure S5 shows the output curves of the 2H- and 1T′-devices with sweeping the control gate and floating gate, respectively. In the first case, all of the devices only have two clear and distinct states, with the control gate increasing from 0 to 15 V, which is ascribed to the weakening of the electrical field of V_{cg} by the stored electrons (holes) in the floating gate. In sweeping the floating gate layer from −1 to 1 V, the obtained linear output curves indicate the realization of good contact.

Figure 3a presents the optical image of the 2H-$MoTe_2$/h-BN heterostructure for the extraction of the tunneling barrier for electrons between the 2H-$MoTe_2$ floating gate and h-BN ($e\phi_{BE}$). The plot of the current density J_T versus the applied voltage V_T is given in Figure 3b, where two tunneling modes (i.e., direct tunneling and Fowler−Nordheim tunneling) are clearly observed. When the voltage drop on the h-BN dielectric satisfies $V_{BN} < \phi_{BE}$, the direct tunneling dominates. In the case of $V_{BN} > \phi_{BE}$, electrons will encounter a triangular barrier and F−N tunneling occurs. The current density in the F−N tunneling regime can be approximately expressed by the following formula:

$$J_{FN} = C_1 E_{h-BN} \exp\left[-\frac{(32m^*_{h-BN})^{1/2}(e\phi_{BE})^{3/2}}{3\hbar e E_{h-BN}}\right] \tag{2}$$

$E_{h\text{-}BN}$, $\hbar$, and e are the electric field in the dielectric, reduced Plank's constant, and the elementary charge, respectively.[51] Figure 3c shows the F−N plot of the 2H-$MoTe_2$/h-BN device. C_1 is determined by the intercept of the F−N plot.

$$C_1 = \frac{e^2 m_e}{32\pi\hbar\phi_{BE} m^*_{h-BN}} \tag{3}$$

where m_e is the free electron mass and $M^*_{h\text{-}BN} = 2.21m_e$ is the effective mass of h-BN.[51−53] Then, the tunnel barrier height for the electron is calculated to be 3.8 eV. Similarly, the tunnel barrier for electrons at the 1T′-$MoTe_2$ floating gate and h-BN is calculated to be 3.9 eV (Figure 3d−f), which is larger than the 2H-$MoTe_2$/h-BN device. Moreover, the high tunnel barrier heights for 2H- and 1T′-$MoTe_2$/h-BN devices are higher than the reported graphene/h-BN device and are related to the work functions of 2H-$MoTe_2$ and 1T′-$MoTe_2$ nanoflakes; this will be discussed later.[53] The thickness of the h-BN nanoflakes for 2H-$MoTe_2$/h-BN and 1T′-$MoTe_2$/h-BN heterostructures are both ∼10 nm. The voltage values at which F−N tunneling occurs can be obtained from Figure 3b,e, and they are 5.0 and 5.5 V, corresponding to the electric field strength of 5.0 and 5.5 MV cm^{-1}, respectively. In the graphene/h-BN device reported before, the critical electrical field between the direct tunneling and F−N tunneling is about 3.6 MV cm^{-1} smaller than those in 2H-$MoTe_2$/h-BN and 1T′-$MoTe_2$/h-BN devices, which is consistent with their extracted tunnel barrier heights.[53] Figure 3g illustrates the band diagram; when applying a positive electrical pulse on the control gate in the 2H-device, the device is in the "Program" state. Electrons tunnel from the MoS_2 channel to the 2H-$MoTe_2$ floating gate layer and then are blocked by the h-BN barrier. When the external electric field is removed, the stored charge in the floating gate layer provides an effective electric field to the MoS_2 channel, helping to maintain its high resistance state. Figure 3h shows the band diagram of the 2H-device with the application of a negative electrical pulse on the control gate. At this time, the device is in the "Erase" state since electrons tunnel back from the 2H-$MoTe_2$ floating gate to the MoS_2 channel with the help of the external field, eliminating the effective electric field provided by the trapped electrons. When the external electric field is removed, the MoS_2 channel will return to the low resistance state. Figure 3i,j depicts the band diagram of the 1T′-device in different states, which are similar to the 2H-device.

It is worth pointing out that the semiconducting multilayer 2H-$MoTe_2$ has a considerable bandgap of ∼1.0 eV, while its conduction and valence bands for metallic 1T′-$MoTe_2$ overlapped. We further measured the work functions of 2H-$MoTe_2$ and 1T′-$MoTe_2$ nanoflakes by Kelvin probe force microscopy (KPFM). The multilayer 1T′-$MoTe_2$ and 2H-$MoTe_2$ nanoflakes were mechanically exfoliated onto the SiO_2/Si substrates covered by chromium/gold (Cr/Au: 8/100 nm). Figure S6a,b,d,e depicts the thicknesses and surface potential differences between the gold substrate and 2H-$MoTe_2$/1T′-$MoTe_2$, respectively. The uniform surface potential energy distribution presented in Figure S6c,f indicates that the

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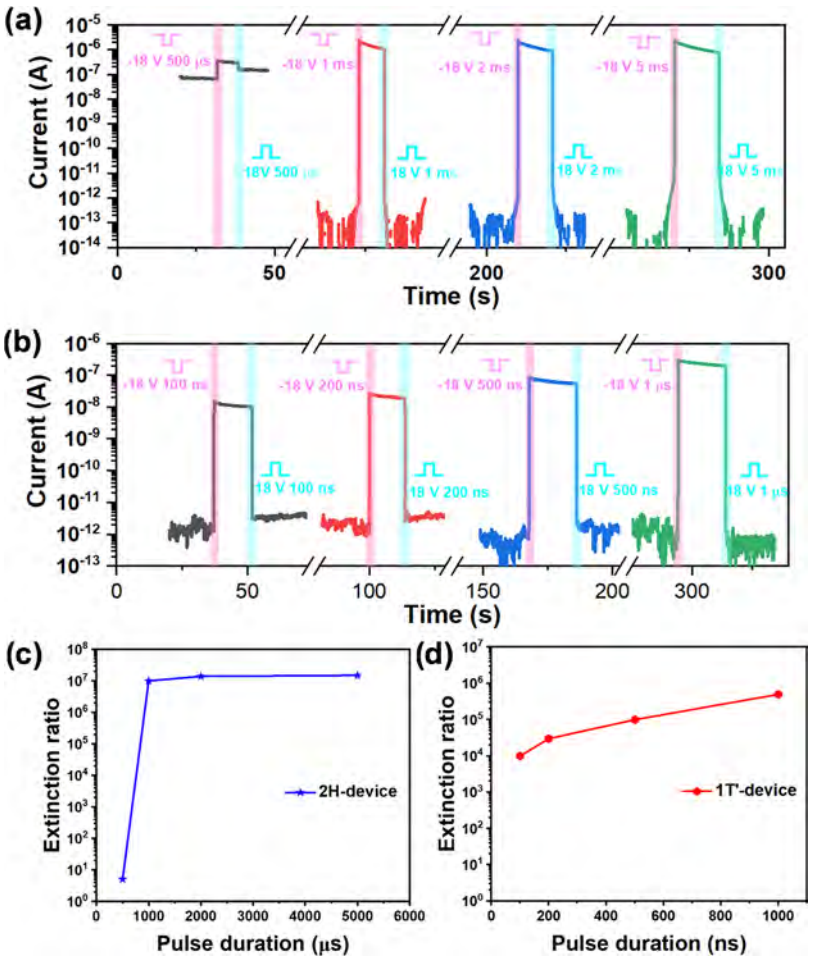

Figure 4. Switching speed of 2H- and 1T′-devices under an electrical pulse with the readout bias of 100 mV. (a) Switching between the Program and Erase states of the 2H-device under ±18 V control gate voltage pulses with the pulse duration increasing from 500 μs to 5 ms. (b) Switching of the Program and Erase states of the 1T′-device under ±18 V control gate voltage pulses with the pulse duration increasing from 100 ns to 1 μs. (c) Extinction ratio of the 2H-device under ±18 V control gate voltage with the pulse duration increasing from 500 μs to 5 ms. (d) Extinction ratio of the 1T′-device under ±18 V control gate voltage with the pulse duration increasing from 100 ns to 1 μs.

materials are homogeneous and the measurement results are credible. Based on the results, it can be concluded that the work function of 1T′-$MoTe_2$ is 0.18 eV higher than that of 2H-$MoTe_2$, which is consistent with other reports.[54] The distinctly different electrical properties of these two materials originate from the different crystal phases. Figure S7a,b shows the crystal structure of the 2H-$MoTe_2$, Mo atoms located at the center, with Te atoms around it to form a hexagonal space group. Figure S7c,d shows the crystal structure of 1T′-$MoTe_2$. Different from the semiconducting phase, in this case, Te atoms locate at the octahedral coordination around the Mo atoms in each layer with a lattice distortion to develop a monoclinic space group. HRTEM images of the atomic arrangement of specific materials are shown in Figure S8.

Compared with 2H-$MoTe_2$, there are more free electrons in metallic 1T′-$MoTe_2$ due to the energy band overlapping, which can provide more carriers tunneling through the h-BN layer. In addition, the tunneling probability of carriers is highly dependent on the energy barrier's height, shape, and thickness.[55] The larger tunnel barrier means that electrons can be preserved longer, which is beneficial to long-term data storage.

Figure 4a shows device performance using ±18 V control gate voltage pulses with different pulse duration to switch the Program and Erase states of the 2H-device. Using a larger pulse voltage to switch the states can make the device work more stably. When the pulse durations are larger than 1 ms, the +18 V pulse can easily switch the device from a high resistance state to a low resistance state and vice versa with a −18 V pulse. And the maximum extinction ratio of the device can exceed 10^7. This value is close to that of other reported 2D flash memory devices using graphene as the floating gate layer. When the pulse duration further drops to 500 μs, switching between the Program and Erase states is hard to achieve. Figure 4b shows the switching performance for the 1T′-device. The electrical pulse amplitude applied on the control gate was kept at ±18 V. The waveforms of the ultrafast programming electrical pulses with different pulse widths ranging from 100 ns to 1 μs are given in Figures S9 and S10. When the pulse duration is only 1 μs, an extinction ratio of 10^6 could be achieved. Even when the pulse duration is further shortened to 100 ns, the switching between the Program and Erase states can still be realized with the extinction ratio approaching 10^4. This ultrafast switching speed between high and low resistance states surpasses most existing vdW heterostructure-based nonvolatile flash memory devices.[18,19,44,50,56] In Table S1, we summarized and compared the flash memory performance based on other 2D materials and our MoS_2/h-BN/1T′-$MoTe_2$

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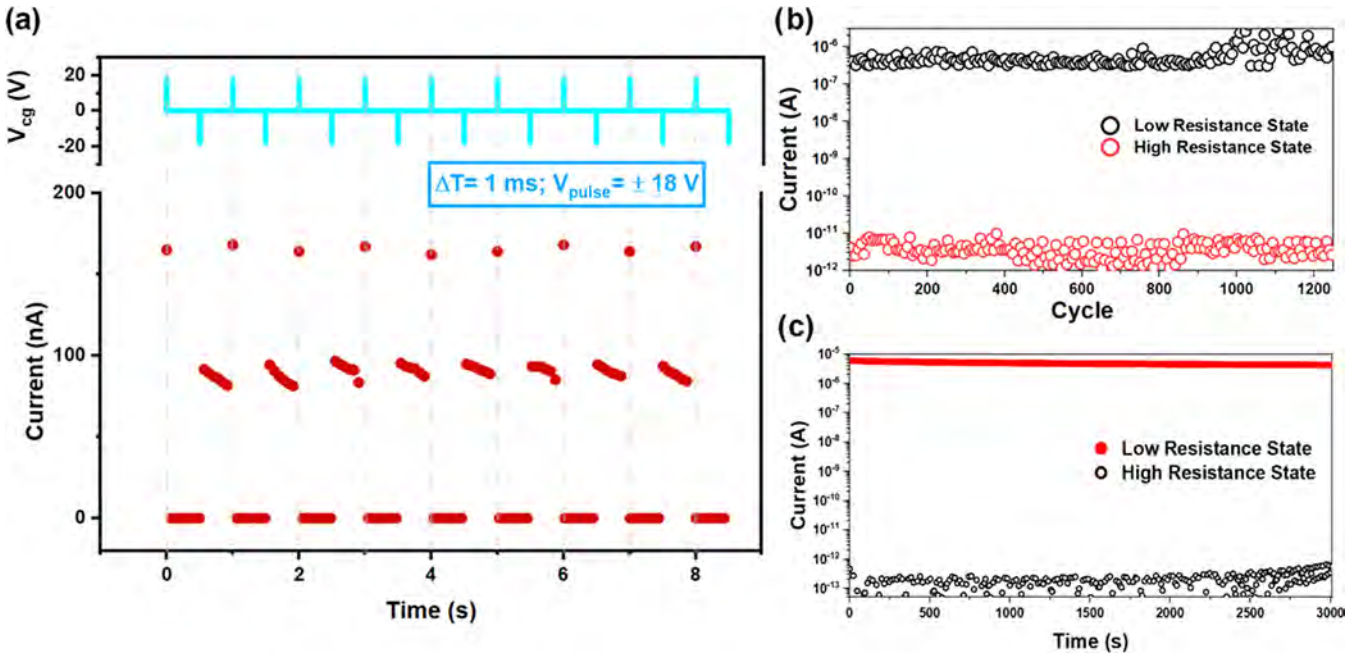

Figure 5. Cycle and retention stability of the 1T′-device under an electrical pulse with the readout bias of 100 mV. (a) Cycle test of the 1T′-device under the ±18 V control gate voltage pulse with a 1 ms pulse duration. (b) Cycle stability of the 1T′-device under the ±15 V control gate voltage pulses with a pulse duration of 1 ms. (c) Long-term stability of the 1T′-device under the ±20 V control gate voltage pulses with a pulse duration of 1 s. By fabricating MoS_2/h-BN/1T′-$MoTe_2$ and MoS_2/h-BN/2H-$MoTe_2$ vdW heterostructure-based memory devices, we comprehensively studied the crucial role of the crystal phase of the floating gate $MoTe_2$ in determining 2D flash memory performance and concluded that 1T′-$MoTe_2$ can significantly improve the device performance including a larger memory window, nanosecond switching speed (100 ns), a higher extinction ratio (10^7), and long cycle (>1200 cycles) and retention (>3000 s) stability compared with its semiconducting counterpart.

heterostructure. It can be found that compared with most reported 2D flash memory devices with considerable cycle and retention stability, the MoS_2/h-BN/1T′-$MoTe_2$ heterostructure presents a much faster switching speed. On the other hand, compared with other 2D flash memory devices with switching speed in tens of nanoseconds, our MoS_2/h-BN/1T′-$MoTe_2$ heterostructure shows superiority in terms of the cycle and retention stability. Figure 4c,d further compares the relationship between the pulse duration and extinction ratio for 2H- and 1T′-devices at the control gate pulses of +18 V. Figure S11 shows the optical images of Hall devices for 2H- and 1T′-$MoTe_2$ nanoflakes. From the Hall measurements at room temperature, the obtained free electron concentrations for 2H- and 1T′-$MoTe_2$ nanoflakes are 9.010×10^{17} cm^{-3} and 1.423×10^{20} cm^{-3}, and the carrier mobilities are 41.5 cm^2 V^{-1} s^{-1} and 58.2 cm^2 V^{-1} s^{-1}, respectively. The faster operation speed of the 1T′-device can be attributed to the much higher free carrier concentrations than the 2H-device.

The cycle and retention measurements of 1T′-$MoTe_2$ were also conducted to demonstrate its high stability and application prospect. As shown in Figure 5a, after applying the control gate voltage pulse of ±18 V/1 ms, the device can successfully realize the continuous switching between Program and Erase states. As shown in Figure 5b, cycle tests were performed to verify the cycle endurability of the 1T′-device, indicating the excellent cycle durability of the 1T′-device. Figure 5c shows the long-term retention stability test over 50 min. The 1T′-device can maintain the stable high and low resistance states for a long time after applying the 20 V/1 s control gate voltage pulses. More importantly, the extinction ratio approaches 10^8, which is superior to most 2D material-based flash memory devices (Table S1). This impressive long-term retention stability can be explained by the larger barrier difference between the floating gate and h-BN, resulting in better preservation of the trapped electrons in the floating gate.

In addition, the 1T′-device also exhibits optical memory behavior. A 532 nm laser was used to demonstrate the optical Erase behavior on the 1T′-device after realizing the Program states by the electrical pulse. Figure S12a illustrates the schematic illustration of the optical programming process. Figure S12b shows the current evolution of the device under the 532 nm laser irradiation. The result proves that the 1T′-device can perform stable multistage Erase behavior by applying a laser pulse train with a frequency of 0.1 Hz and a duty ratio of 1% (t_{pulse} = 10 ms). It demonstrates that the optical pulse train can successfully achieve stable multilevel programming states on our memory device. As shown in Figure S12c,d, the 1T′-device can realize more diverse multistage regulation by tuning the laser powers and frequencies. It suggests that our 1T′-device presents a high potential for future multifunctional flash memory with both electronic and optical memory. Figure S12e−g explains the working mechanism behind the optical memory. Figure S12e shows the Program state under the positive control gate voltage pulse. Figure S12f shows the band diagram in the dark; in this case, the 1T′-$MoTe_2$ floating gate stores a large number of electrons. When the laser pulses are irradiated on the device, considerable photogenerated electron/hole pairs will be induced in the semiconducting channel, which is shown in Figure S12g. Since holes are easier to tunnel through the h-BN insulating layer than electrons, more holes tunnel into the floating gate layer to recombine with the stored electrons, resulting in a reduced net charge in the floating gate layer.[57]

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With the number of optical pulses increasing, optical-induced multilevel switching states can be obtained.

3. CONCLUSIONS

In summary, we comprehensively explored the impact of the crystal phase on the performance of the nonvolatile flash memory devices fabricated from $MoTe_2$-based 2D vdW heterostructures. Specifically, MoS_2/h-BN/1T′-$MoTe_2$ and MoS_2/h-BN/2H-$MoTe_2$ heterostructures were fabricated on the SiO_2/Si substrate, where the few-layer 2H-MoS_2 nanoflake was used as the semiconducting channel, the multilayer h-BN nanoflake was used as the tunnel dielectric, and $MoTe_2$ nanoflakes in the metallic or semiconducting phase were used as the charge-trapping layer. SiO_2/Si served as the gate dielectric and control gate. After comparing the device performance, it is concluded that the 1T′-device exhibits a much better performance than that of the 2H-device, including a larger memory window, a much faster switching speed of ∼100 ns, and a higher extinction ratio of $\sim 10^7$. The much better memory performance obtained in the 1T′-device can be explained by the differences of work function, free carrier concentration, and carrier mobility between the 1T′-$MoTe_2$ and 2H-$MoTe_2$ nanoflakes. Moreover, the 1T′-device also exhibited excellent cycle and retention stability. Interestingly, the 1T′-device also presents optically programmed memory behavior. Our study clearly uncovers that 2D 1T′-phase TMDs could serve as the floating gate for the fabrication of high-performance flash memory devices. The design and fabrication of flash memory devices based on 1T′-phase TMDs may pave a new avenue for the development of 2D material-based electronics in the future.

4. EXPERIMENTAL SECTION

4.1. Device Fabrication. Single crystals of 2H-MoS_2, h-BN, 2H-$MoTe_2$, and 1T′-$MoTe_2$ were purchased from 2D Semiconductor Inc. All nanoflakes used in fabricating the device in this work were obtained through mechanical exfoliation methods. The insulating layer and channel material were stacked on top of the floating gate material in sequence via a dry transfer method. Poly(dimethylsiloxane) (PDMS) was used as the transfer medium. The electrodes were patterned by electron beam lithography (EBL), followed by the thermal evaporation of 8 nm Cr and 60 nm Au. In the end, the devices were obtained after the standard lift-off process.

4.2. Device Characterizations. The optical images of these devices were captured by an optical microscope (Nikon, ECLIPSE LV100ND). The height profiles of the vdW nanoflakes in these heterostructures were characterized by the atomic force microscope (AFM) (Bruker, Dimension Icon with Scan Asyst). The work function of the multilayer nanoflakes is measured by Kelvin probe force microscopy (KPFM). The Raman spectra of the different regions in the heterostructure were obtained by a Renishaw Raman microscope with the excitation of a 532 nm polarized laser at room temperature. The electrical performance of these devices was characterized by the Agilent 4155 C semiconductor analyzer (Agilent Technologies, Santa Clara, CA). The electrical pulse was generated by a B1500A semiconductor device parameter analyzer system equipped with a high-voltage semiconductor pulse generator unit. The waveforms of the ultrafast electrical pulses were recorded by a digital oscilloscope (Tektronix TBS 1102B-EDU). A homemade optoelectronic characterization platform measured the optical pulse-triggered conductance evolution of the devices at the ambient conditions, where the 532 nm laser was provided by a monochrome laser and guided to the device via an optical fiber; the triggered current was monitored by the aforementioned Agilent 4155 C semiconductor analyzer.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsami.3c06316.

Fabrication process of a typical 2D vdW heterostructure nonvolatile flash memory device; STEM image and EDS mapping of the cross section of the device; AFM measurements of the 2H-device and 1T′-device; output curves of 2H- and 1T′-devices; KPFM measurements of 2H- and 1T′-$MoTe_2$ nanoflakes; schematic illustration of crystal structures of 2H- and 1T′-$MoTe_2$; crystal structures of 2H- and 1T′-$MoTe_2$; waveforms of ultrafast programming/erasing electrical pulses with different pulse widths; optical images of the Hall device; and optical memory of the 1T′-device (PDF)

AUTHOR INFORMATION

Corresponding Author

Chaoliang Tan − *Department of Electrical Engineering, City University of Hong Kong, Kowloon 999077 Hong Kong SAR, China; Department of Chemistry and Center of Super-Diamond and Advanced Films (COSDAF), City University of Hong Kong, Kowloon 999077 Hong Kong SAR, China; Department of Electrical and Electronic Engineering, The University of Hong Kong, Pokfulam 999077 Hong Kong SAR, China;* orcid.org/0000-0003-1695-5285; Email: chaoltan@cityu.edu.hk, cltan@hku.hk

Authors

Yunpeng Xia − *Department of Electrical Engineering, City University of Hong Kong, Kowloon 999077 Hong Kong SAR, China*

Jiajia Zha − *Department of Materials Science and Engineering, City University of Hong Kong, Kowloon 999077 Hong Kong SAR, China*

Haoxin Huang − *Department of Electrical Engineering, City University of Hong Kong, Kowloon 999077 Hong Kong SAR, China*

Huide Wang − *Department of Electrical Engineering, City University of Hong Kong, Kowloon 999077 Hong Kong SAR, China; Department of Materials Science and Engineering, City University of Hong Kong, Kowloon 999077 Hong Kong SAR, China*

Peng Yang − *College of Integrated Circuits and Optoelectronic Chips, Shenzhen Technology University, Shenzhen 518118, China*

Long Zheng − *Department of Chemistry, The Chinese University of Hong Kong, Shatin 999077 Hong Kong SAR, China*

Zhuomin Zhang − *Department of Mechanical Engineering, City University of Hong Kong, Kowloon 999077 Hong Kong SAR, China*

Zhengbao Yang − *Department of Mechanical Engineering, City University of Hong Kong, Kowloon 999077 Hong Kong SAR, China; Department of Mechanical and Aerospace Engineering, Hong Kong University of Science and Technology, Kowloon 999077 Hong Kong SAR, China*

Ye Chen − *Department of Chemistry, The Chinese University of Hong Kong, Shatin 999077 Hong Kong SAR, China;* orcid.org/0000-0003-0821-7469

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Hau Ping Chan − *Department of Electrical Engineering, City University of Hong Kong, Kowloon 999077 Hong Kong SAR, China*

Johnny C. Ho − *Department of Materials Science and Engineering, City University of Hong Kong, Kowloon 999077 Hong Kong SAR, China;* orcid.org/0000-0003-3000-8794

Complete contact information is available at: https://pubs.acs.org/10.1021/acsami.3c06316

Author Contributions

◆Y.X. and J.Z. contributed equally to this work. The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

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